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<u>L6</u>	L5 same (embedded or on-chip)	15	<u>L6</u>
<u>L5</u>	L1 same probe	232	<u>L5</u>
<u>L4</u>	L3 same l2 same l1	0	<u>L4</u>
<u>L3</u>	probe adj1 point	1003	<u>L3</u>
<u>L2</u>	probe adj1 line	421	<u>L2</u>
<u>L1</u>	logic adj1 analyzer	1005	<u>L1</u>

END OF SEARCH HISTORY

Ton, David

From: JWGluck@venable.com
Sent: Monday, September 22, 2003 2:24 PM
To: David.Ton@uspto.gov
Cc: JWGluck@venable.com
Subject: RE: New Proposed Claims

Hi, David.

Thank you for your very thoughtful and detailed reply! We really appreciate this!

I will forward your proposal to the inventors and find out what they think.

Thank you, again!

Best regards,

Jeff

-----Original Message-----

From: David.Ton@USPTO.GOV [mailto:David.Ton@USPTO.GOV]
Sent: Monday, September 22, 2003 2:19 PM
To: Gluck, Jeffrey W., Ph.D
Subject: RE: New Proposed Claims

Hi Jeff,

I think "selectively enable probe points" is well known. People used to selectively move the probe point around the logic circuit to probe the state of a node in the circuit for diagnostic.

Therefore, I propose to add the analysis engine into the claim to make all the elements linking together since the the analysis engine is the heart of the invention.

In addition, during the interview with the applicant, he said that his invention is distinguish from the prior art by using hardware instead of software to enable the signal path by "coupling said signal paths to the channels of said analysis engine and turning on enabling circuits".

The following is a proposal for claim 1:

1. (Currently Amended) An integrated circuit comprising:
one or more logic blocks generating one or more system-operation signals at one or more system-operation clock rates;
a control unit for performing test and debug operations of said logic blocks of said integrated circuit;
a memory associated with said control unit, said memory holding instructions for said control unit;
a plurality of probe lines responsive to said control unit for carrying system-operation signals from a set of selectively enabled probe points of said logic blocks, wherein said probe lines comprise strings of storage elements providing signal paths from said probe points to said memory; and

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an analysis engine implemented in the form of an on-chip logic analyzer for capturing sequential snapshots of sets of said system-operation signals, the logic analyzer having channels which are formed from said probe lines to move data captured at a probe point towards the end of the logic analyzer channel where data are stored in said memory as sets of system operation signals so that said sets of system-operation signals are retrievable,

wherein the set of selectively enabled probe points are selected from a set of pre-existing probe points by coupling said signal paths to the channels of said analysis engine and turning on enabling circuits, and wherein said signal paths are capable of moving sets of said system-operation signals at at least one of said system-operation clock rates.

Jeff, if you agree with my proposal, please amend claims 10 and 15 yourself.

Best regards,

David

[Ton, David] -----Original Message-----

From: JWGluck@venable.com [mailto:JWGluck@venable.com]

Sent: Friday, September 12, 2003 8:48 AM

To: David.Ton@uspto.gov

Cc: JWGluck@venable.com

Subject: RE: New Proposed Claims

Thanks, David.

I look forward to hearing from you sometime next week.

Best regards,

Jeff

-----Original Message-----

From: David.Ton@USPTO.GOV [mailto:David.Ton@USPTO.GOV]

Sent: Thursday, September 11, 2003 2:13 PM

To: Gluck, Jeffrey W., Ph.D

Subject: RE: New Proposed Claims

Hi Jeff,

Tomorrow is my day off. I will consider your proposed claims next week.

Have a nice week end,

David

-----Original Message-----

From: JWGluck@venable.com [mailto:JWGluck@venable.com]
Sent: Wednesday, September 10, 2003 4:02 PM
To: David.Ton@uspto.gov
Cc: JWGluck@venable.com
Subject: New Proposed Claims

Hi, David.

I have read your arguments, and I have also conferred with the client. While we do not agree with your position, we appreciate that you appear to be standing by that position. In order to try to speed things up, therefore, we have decided to propose further amendments to the claims, which can be found in the attached file.

To briefly summarize, in the new proposed claims, we have attempted to differentiate the present invention from Veenstra by including a limitation that only a subset of pre-existing probe points are selected for use. Veenstra can not do this because Veenstra's system does not exist until it (i.e., the PLD) is programmed. That is, there are no pre-existing probe points in Veenstra to selectively enable, unlike in the present invention. In Veenstra, the probe points are created by the program.

I look forward to hearing what you think about this.

Best regards,

Jeff

<<Proposed Claims - 41567-192232_v3.DOC>>

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